CLAIMS

What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A method of preventing a short from occurring in a gate stack during a self-align contact etch process, comprising:

providing a device having at least two adjacent gate stacks, wherein at least one of said adjacent gate stacks is separated from a vertical nitride spacer by a vertical oxide spacer;

creating a space by removing an upper portion of said vertical oxide spacer; and

forming a nitride layer over said memory device, such that at least a portion of said space is filled by said nitride layer.

2. The method of claim 1, wherein said vertical oxide spacer is between about 50Å and about 300Å in thickness.

3. The method of claim 2, wherein said vertical oxide spacer is between about 100Å and about 200Å in thickness.

4. The method of claim 1, wherein said nitride layer has a thickness equal to about one half the width of said vertical oxide spacer.

5. The method of claim 1, wherein said removing is achieved by contacting said vertical oxide spacer with an HF solution.

6. The method of claim 5, wherein said HF solution is an aqueous solution.

7. The method of claim 1, wherein said removing is by etching.

8. The method of claim 1, wherein said at least one gate stack is a flash cell gate stack.

9. A memory device comprising:

a gate stack;

a vertical oxide spacer adjacent to said gate stack; and

a continuous nitride layer overlaying said vertical oxide spacer and said gate stack.

10. The memory device of claim 9, wherein said gate stack comprises a floating gate and a control gate.

11. The memory device of claim 9, wherein said vertical oxide spacer is between about 50Å and about 300Å in thickness.

12. The memory device of claim 11, wherein said vertical oxide spacer is about 100Å and about 200Å in thickness.

13. The memory device of claim 9, wherein said nitride layer has a thickness equal to about one half the width of said vertical oxide spacer.

14. A memory device comprising:

a gate stack;

a vertical spacer adjacent to said gate stack, wherein said vertical spacer has a lower portion comprising an oxide and an upper portion comprising a nitride; and

a continuous nitride layer overlaying said vertical spacer and said gate stack.

15. The memory device of claim 14, wherein said vertical oxide spacer is between about 50Å and about 300Å in thickness.

16. The memory device of claim 15, wherein said vertical oxide spacer is between about 100Å and about 300Å in thickness.

17. The memory device of claim 14, wherein said nitride layer has a thickness equal to about one half the width of said vertical oxide spacer.

18. The memory device of claim 14, wherein said gate stack is a flash cell gate stack.

19. A method of fabricating a memory device, comprising:

forming a tunnel oxide layer on a substrate;

forming a floating gate layer over said tunnel oxide layer;

forming an oxide/nitride/oxide layer over said floating gate layer;

forming a control gate layer over said oxide/nitride/oxide layer;

forming a silicide layer over said control gate;

forming a cap over said silicide layer to form a gate stack;

forming a continuous oxide layer over said gate stack and said substrate, said continuous oxide layer having horizontal and vertical surfaces;

removing the horizontal surfaces of said continuous oxide layer;

forming a first continuous nitride layer over said gate stack, said vertical oxide surfaces and said substrate, said first continuous nitride layer having horizontal and vertical surfaces, with each said vertical oxide surface thereby becoming an oxide spacer;

removing the horizontal surfaces of said first continuous nitride layer, thereby exposing each said oxide spacer at its top end;

removing a portion of said oxide spacer from its top end; and

depositing an amount of nitride sufficient to replace the removed portion.

20. The method of claim 19, wherein said silicide layer comprises tungsten.

21. The method of claim 19, wherein said floating gate layer comprises a polysilicon.

22. The method of claim 19, wherein said control gate layer comprises a polysilicon.

23. The method of claim 19, wherein said oxide/nitride/oxide layer comprises a silicon nitride layer interposed between two silicon dioxide layers.

24. The method of claim 19, wherein said cap comprises nitride.

25. The method of claim 19, wherein said step of forming said cap comprises the step of providing TEOS.

26. The method of claim 19, wherein said continuous oxide layer comprises TEOS.

27. The method of claim 19, wherein said continuous oxide layer is between about 50Å and 300Å in thickness.

28. The method of claim 27, wherein said continuous oxide layer is between about 100Å and about 200Å in thickness.

29. The method of claim 19, wherein said removing the horizontal surfaces of said continuous oxide layer is by a first etch process.

30. The method of claim 29, wherein said first etch process is a dry etch process.

31. The method of claim 19, wherein said removing the horizontal surfaces of said first continuous nitride layer is by a second etch process.

32. The method of claim 31, wherein said second etch process is a dry etch process.

33. The method of claim 19, wherein said removing is by contacting the exposed top end of the vertical oxide spacer with an HF solution.

34. The method of claim 33, wherein said HF solution is an aqueous solution.

35. The method of claim 19, wherein said removing includes etching.

36. A memory device comprising:

a gate stack comprising:

a tunnel oxide layer on a substrate;

a floating gate layer over said tunnel oxide layer;

an oxide/nitride/oxide layer over said floating gate layer;

a control gate layer over said oxide/nitride/oxide layer;

a silicide layer over said control gate layer;

a cap over said silicide layer;

a vertical spacer adjacent to said gate stack, wherein said vertical spacer has a lower portion comprising an oxide and an upper portion comprising a nitride; and

a continuous nitride layer overlaying said vertical spacer and said gate stack.

37. The memory device of claim 36, wherein said silicide layer comprises tungsten.

38. The memory device of claim 36, wherein said floating gate layer comprises a polysilicon.

39. The memory device of claim 36, wherein said control gate layer comprises a polysilicon.

40. The memory device of claim 36, wherein said oxide/nitride/oxide layer comprises a silicon nitride layer interposed between two silicon dioxide layers.

41. The memory device of claim 36, wherein said cap comprises nitride.

42. The memory device of claim 36, wherein said cap comprises TEOS.

43. The memory device of claim 36, wherein said oxide portion comprises TEOS.

44. The memory device of claim 36, wherein said vertical spacer is between about 50Å and 300Å in thickness.

45. The memory device of claim 44, wherein said vertical spacer is about 100Å and 200Å in thickness.

46. The memory device of claim 36, wherein said continuous nitride layer has a thickness equal to about one half the width of said vertical spacer.

47. A memory device comprising:

a gate stack comprising:

a tunnel oxide layer on a substrate;

a control gate layer over said tunnel oxide layer;

a silicide layer over said control gate layer;

a cap over said silicide layer;

a vertical spacer adjacent to said gate stack, wherein said vertical spacer has a lower portion comprising an oxide and an upper portion comprising a nitride; and

a continuous nitride layer overlaying said vertical spacer and said gate stack.

48. A method of fabricating a memory device, comprising:

forming a tunnel oxide layer on a substrate;

forming a control gate layer over said tunnel oxide layer;

forming a silicide layer over said control gate layer;

forming a cap over said silicide layer to form a gate stack;

forming a continuous oxide layer over said gate stack and said substrate, said continuous oxide layer having horizontal and vertical surfaces;

removing the horizontal surfaces of said continuous oxide layer;

forming a first continuous nitride layer over said gate stack, said vertical oxide surfaces and said substrate, said first continuous nitride layer having horizontal and vertical surfaces, with each said vertical oxide surface thereby becoming an oxide spacer;

removing the horizontal surfaces of said first continuous nitride layer, thereby exposing each said oxide spacer at its top end;

removing a portion of said oxide spacer from its top end; and

depositing an amount of nitride into said removed portion sufficient to replace the removed portion.

49. A method of fabricating a memory device, comprising:

forming a continuous oxide layer over a gate stack positioned on a substrate, said continuous oxide layer having horizontal and vertical surfaces;

removing the horizontal surfaces of said continuous oxide layer;

forming a first continuous nitride layer over said gate stack, said vertical oxide surfaces and said substrate, said first continuous nitride layer having horizontal and vertical surfaces, with each said vertical oxide surface thereby becoming an oxide spacer;

removing the horizontal surfaces of said first continuous nitride layer, thereby exposing each said oxide spacer at its top end;

removing a portion of said oxide spacer from its top end; and

depositing an amount of nitride into said removed portion sufficient to replace the removed portion.

50. The method of claim 49, wherein said continuous oxide layer comprises TEOS.

51. The method of claim 49, wherein said continuous oxide layer is between about 50Å and 300Å in thickness.

52. The method of claim 51, wherein said continuous oxide layer is between about 100Å and about 200Å in thickness.

53. The method of claim 49, wherein said removing is by contacting the exposed top end of the vertical oxide spacer with an HF solution.

54. The method of claim 49, wherein said vertical oxide spacer is between about 50Å and about 300Å in thickness.

55. The method of claim 54, wherein said vertical oxide spacer is between about 100Å and about 200Å in thickness.

56. The method of claim 54, wherein said nitride layer has a thickness equal to about one half the width of said vertical oxide spacer.

57. A processor system comprising:

a processor; and

a memory device coupled to exchange data with said processor, said memory device comprising:

a gate stack;

a vertical spacer adjacent to said gate stack, wherein said vertical spacer has a lower portion comprising an oxide and an upper portion comprising a nitride; and

a continuous nitride layer overlaying said vertical spacer and said gate stack.

58. The processor system of claim 57, wherein said vertical oxide spacer is between about 50Å and about 300Å in thickness.

59. The processor system of claim 58, wherein said vertical oxide spacer is between about 100Å and about 300Å in thickness.

60. The processor system of claim 57, wherein said nitride layer has a thickness equal to about one half the width of said vertical oxide spacer.

61. The processor system of claim 57, wherein said gate stack is a flash cell gate stack.